Exhibit

3-3

Serial 9Mb Flash EEPROM for Solid State Disk Applications

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I. INTRODUCTION

A 9Mb Flash EEPROM incorporating a serial interface and other features specifically suited for low cost, high capacity and low power solid state storage systems is described. The chip has been fabricated using a triple polysilicon, single metal 0.9 micron CMOS process with memory cell size of 2.70μ x 2.35μ and die size of 331mils x 516mils^2. Two types of transistors are used: thin oxide transistors are used for low read and programming voltages, and thick oxide transistors are used for high erase voltage. The memory array utilizes a virtual ground architecture with buried n+ source / drain diffusions contacted to metal bit lines every 32 cells. The Flash EEPROM cell erases using inter-poly dielectric tunneling and programs using channel hot electron injection.

The use a of split channel memory transistor allows the floating gate portion of the cell to be erased to negative thresholds, thus eliminating the over-erase limitation of traditional stacked gate flash cells. Figure 1 shows the schematic representation of the memory cell / array and the cell operating voltages under read, program and erase.

II. SERIAL INTERFACE

The memory chip is designed to be used in multi-chip systems with a dedicated controller to perform data transfer from the host to the memory system. Therefore, to lower overall system cost, a serial interface has been developed which minimizes pin count (with all pads on one side of the chip) and provides denser packing of memory chips on a memory card. Also, some of the functions typically performed on the memory chip have been off-loaded to the controller to reduce active chip area and enhance wafer yields.

The serial interface[1] to the chip consists of two inputs (SI0.1, SI1.1), two outputs (SO0.1), a 20 MHz clock (SCLK), chip select (CS) and pointer / data select (PD). Two serial inputs and outputs are used to double the serial data transfer. Figure 2 shows the register model for the memory device. Data entering on the SI0.1 pins is routed to the register which is selected based on the state of the PD pin and the contents of the pointer register (PTRREG). First, when PD is high, the data input SI0.1 are routed into PTRREG. Then, when PD is taken low, the pointer register is considered loaded and the serial inputs are routed to one of the other registers (address, data or command) based on the contents of PTRREG. Finally, PD is taken high again and the selected register is considered loaded. Different commands may require a sequence of multiple registers to be loaded before execution of the command. Commands are executed upon the rising edge of PD following loading of the command register. There are a total of sixteen commands available to acuvate various device functions and test modes.

III. READ PROTOCOL

The memory device is organized as four quadrants of 1152 columns x 2048 rows each. Each quadrant is divided into 512 sectors: each sector consists of 576 bytes: 512 user data bytes (compatible with most operating systems) and 64 bytes of overhead and ECC information.

The read protocol is designed to output data from the device at the maximum rate possible, with no inter-sector delay. Sector data is divided into chunks (64 bits, 32 clock cycles). While one chunk is shifted out, the next input address is shifted in and the associated memory access time is absorbed. The output of the 64 sense amplifiers is loaded in parallel into the data register upon low to high transition of CS (data register load). New data can be shifted out once CS is taken low again. The time require to load new address and memory access time (including row delay) is hidden in the shift out time of the previous chunk. Figure 3 illustrates the read protocol timing.

During read, the selected memory cell current (Ic) is compared against a mirrored reference Flash EEPROM cell current (transistor P1 in Figure 4). Transistor P2 amplifies the compared difference in current while N1 also mirrors the reference current. Together, P2 and N1 translate the small difference in current into a large voltage signal. A highly accurate current sensing scheme is realized with a minimal transistor configuration.

IV. SECTOR ERASE AND PROGRAM

The 512 user data byte sector is the smallest unit of erase. Multiple random sectors or the full chip can be erased in one 1ms high voltage erase pulse generated on chip. Magnitude and duration of the erase pulse are controlled externally. All sectors to be erased must first be 'tagged'. Executing the tag command sets one erase latch through a selected row line (eliminating the need for a separate erase decoder) as illustrated in Figure 5. Parallel erase of all tagged sectors can be accomplished by subsequently executing an erase command and applying an erase voltage pulse. To minimize erase oxide stress and to achieve sector endurance exceeding 100,000 program / erase cycles, sectors verified to be erased are 'untagged' by the controller to prevent further erasure while other sectors (during parallel multiple sector erase) in the group which need additional erase pulses continue to erase. At the end of each pulse, sectors tagged for erase are verified to determine if additional erase pulses are required.

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The memory cell and its operation are optimized for fast programming using 5us pulses. Eight-four bits are programmed in parallel, followed by an on chip verify operation initiated by the controller. The programming voltage (12V) is applied externally.

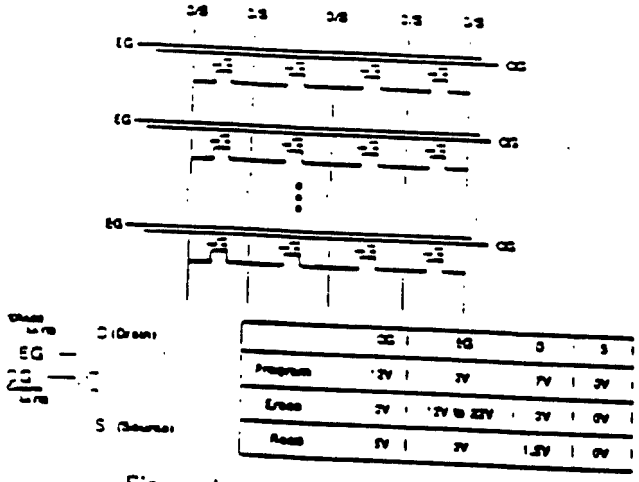

Figure 1 Array Configuration

V. CONCLUSION

A 9Mb Flash EEPROM for high capacity solid state disks is described. A serial protocol and small sector size, fast programming and high sector endurance coupled with a dedicated controller help create a new class of data storage systems.

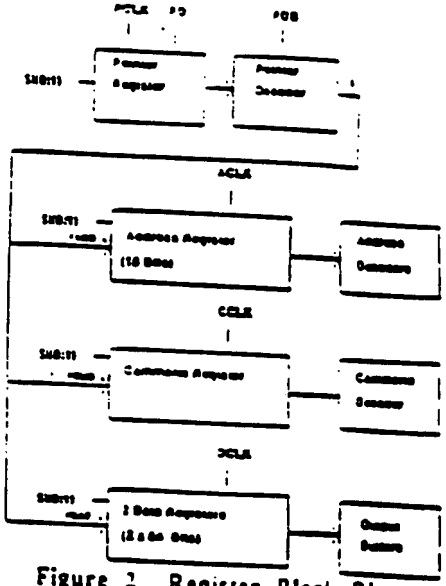

Figure 2 Register Block Diagram

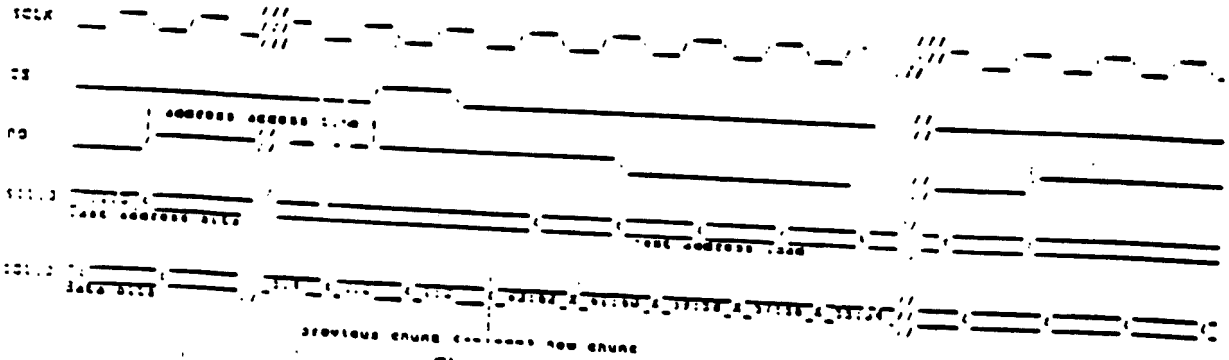

Figure 3 Read Protocol

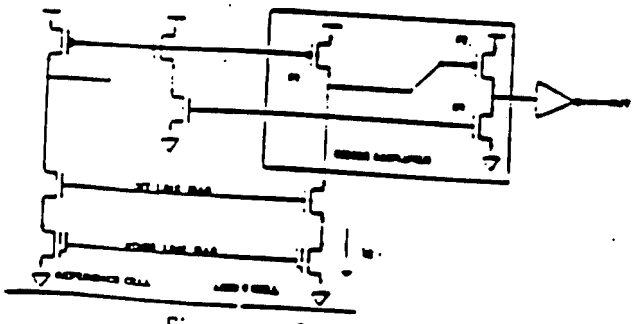

Figure 4 Sense Amplifier

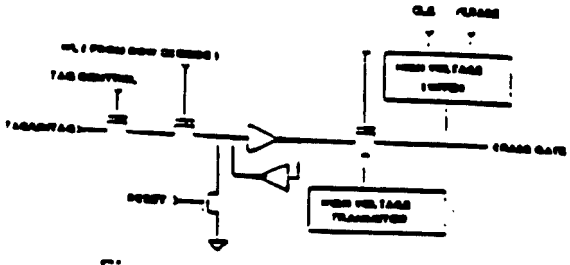

Figure 5 Sector Erase Latch

[2] U.S. Patents pending
[3] U.S. Patents pending